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Effect of Electronic Properties of Si1-xGex and SiC Semiconductors on the Electrical Behavior of MOS Transistors

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Abstract

In this paper, the electrical performance of Metal-Oxide-Semiconductor MOS transistors in $Si_{1-x}Ge_x$ and SiC technologies have been studied by BSIM3v3 model. In which the output charac- teristic $I_D=f(V_{DS})$, transfer characteristic $I_D=f(V_{GS})$ and I_{ON}-I_{OFF} currents of the MOS($Si_{1-x}Ge_x$) transis- tors have been investigated and the results so obtained are compared with the MOS(SiC) transistors, using 130 nm technology and OrCAD PSpice software. This study allowed to know the extent to which the electrical behavior of transistors is affected by the most important electronic properties of semiconductors, and the simulation results showed that the above transistors work properly in a regime under a threshold voltage of about 1.2 V. They can be used in low voltage and low power microelectronics by controlling the germanium x fraction and the polytypes of MOS($Si_{1-x}Ge_x$) and MOS(SiC) transistors respectively.

Keywords: *Si1-xGex; SiC; MOS Transistor; BSIM3v3 Model; 130 nm technology; I-V Characteristics.*

1. Introduction

Search for increasingly enhanced electronic performance, such as speed, low power consumption, etc., requires the use of new components to meet ever increasing demands of telecommunications and multimedia technologies. The use of silicon has shown its limitations in modern telecommunications and in nanometric integrated circuits manufacturing. Reducing transistor size causes degradation in silicon transistors performance and hence a need for alternative solutions [1]. One of such solutions is the use of III-V or IV-IV semiconductors that have better properties than silicon such as mesh size, gap width, carrier mobility, etc.

Band gap engineering has enabled significant advances in component technologies. Germanium, due to its compatibility with the silicon (the two are completely miscible), its lattice mismatch, its band structure, its high mobility of carriers (electrons and holes), its lowest gap with respect to silicon, form with Si the material SiGe. SiGe is introduced intobipolar and CMOS technologies to boost the limits faced by silicon devices [2].

The use of SiGe materials in microelectronic devices needs an understanding of doping impurities diffusion

mechanisms in these alloys in order to master concentration profiles during manufacturing of components. At present, SiGe offers mature processes and

substantial yields to compete with traditional technologies [3].

Thus, SiGe heterojunction bipolar transistors and field effect transistor are good alternatives for power amplification, communication systems and digital circuits requiring high speed, high integration and low cost. The addition of Ge to Si with a fraction x gives Si1-xGex alloys. Their use in electronic and optoelectronic devices has grown considerably due to the additional degrees of freedom it offers in the design and optimization of devices [4]. Many studies have been made on Si1-xGex MOS transistors heterojunctions with very small x values for solar cells [5], modulation,sensors, etc. applications [6]. Recently, SiGe alloy is used to realize integrated circuits with CMOS and BiCMOS technologies like PLL, QVCO, mixer and Low-noise amplifier LNA [7, 8].

In addition, many materials have been proposed to replace silicon technology, among these materials Silicon Carbide (SiC) [9], this is due to their distinctive characteristics such as wide bandgap, high thermal conductivity, high breakdown field and high saturation velocity of electrons Table 1 [10]. This is why it is used in the manufacture of electronic devices with high-voltage, high-power, high-frequency and which operate within a wide range of temperature [11]. The SiC is characterized by many polytypes [10], the most important and most commonly used of which in electronic applications are 3C-SiC, 4H-SiC and 6H-SiC. In addition to using this technology in the MOSFET transistors, they were also used to manufacture the high- voltage and high-power DG-MOSFET transistors [9, 12, 13] or in the form of SiC/SiO2 layer in these transistors [14, 15]. In the last few years, research has shown that the submicron electronic devices in SiC technology work well in low voltage and low power [16–19].

In this paper, we will study, characterize and compare the electrical behavior of MOS transistors in Si1-xGex and SiC technologies with submicron scale 130nm using the BSIM3v3 (Berkeley Short-Channel IGFET Model) model and Orcad(PSpice) software as a simulation tool by studying the most important static characteristics (Output characteristic ID=f(VDS) and Transfer characteristic ID=f(VGS) as well as the ION and IOFF currents. On the basis of determined equations, components are simulated for five values of Ge x fraction (x = 0, x = 0.25, x = 0.5, x = 0.75 and x = 1) for MOS(Si1-xGex) transistors. Two extreme cases, x = 0 and x = 1, corresponding to pure silicon and pure germanium materials are used to set the model. This interval of x is used to study evolution of various electronic characteristics of MOS(Si1-xGex) transistors as a function of germanium x fraction. For MOS(SiC) transistors, we will simulate three MOS transistors in 3C-SiC, 4H-SiC and 6H-SiC technologies. Then we will carry out a comparative study between MOS(Si1-xGex) and MOS(SiC) transistors.

2. MOS Transistor structure

In this work, we will use the structure of MOS transistors in Si1-xGex and SiC technologies of Figure .1 to perform the calculations in order to establish the model and do the simulation.

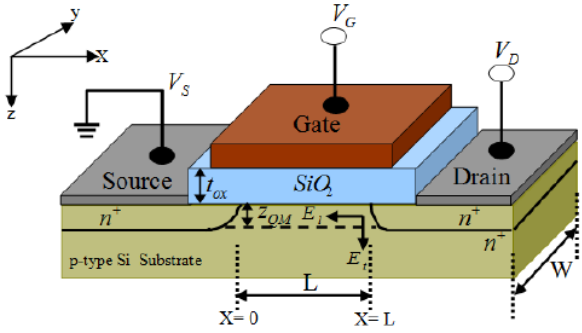


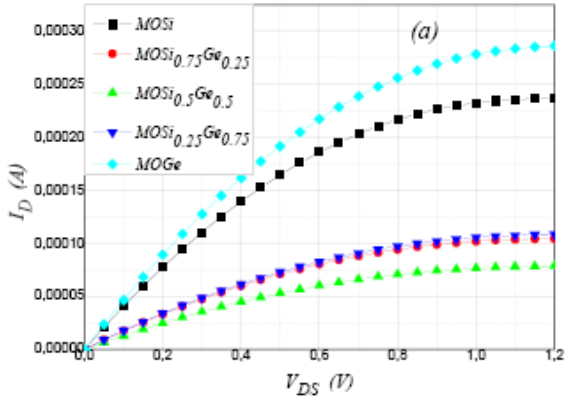
Figure 1. Structure used of MOS(Si1-xGex) and MOS(SiC) transistors.

The transistors are identical from the point of view of constitution. They differ only in the nature of the semiconductor material. The doping of the source, the drain and the gate is of the order of 1020cm-3 for the two transistors. That of the Nch channel, it is equal to 2.3549 ×1017cm-3 [20]. The doping of substrates Nsub is equal to 6 ×1016cm-3. In our study, we opted for limiting dimensions allowed by the BSIM3v3 model of the MOSFET transistor [21] (length of the channel L=130nm and its width W=160nm). To realize the 130nm technology, it is necessary to use an oxide layer of thickness Tox=2.3nm, and a polarization of a value VDD = 1.2V [22]. For the PSpice simulation of the BSIM3v3 MOS transistor, we will use level 7 [23].

3. Results and discussion

In order to study the influence of the fraction x on MOS transistors in SiGe technologies and the type of polytypes on silicon carbide transistors, we simulated five MOS(Si1-xGex) transistors with respectively x=0 , 0.25, 0.5, 0.75 and 1, and three MOS(SiC) transistors (3C-SiC, 4H-SiC and 6H-SiC).

To characterize these transistors in direct polarization mode, we have applied a voltage VGS of 1.2V and varied VDS from 0 to 1.2V. The voltage values of VDS were chosen so as to distinguish the two regions of operation (linear and saturation). Figure 2 shows the evolution of ID drain current as a function of VDS drain voltage of the MOS transistors in Si1-xGex and SiC technologies at room temperature.



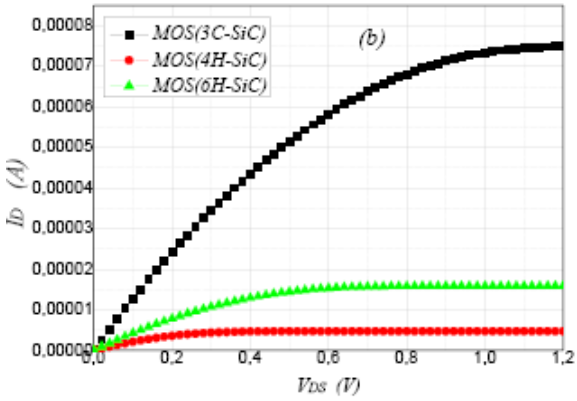


Figure 2: Output characteristic of MOS transistors: a) in Si1-xGex and b) in SiC.

Drain current of MOS(Si1-xGex) transistors decreases with Ge fraction x from $x = 0$ (Silicon transistor) to $x = 0.5$, then increases with $x > 0.5$ to $x = 1$ (Germanium transistor) as shown in Figure 3. MOS(Si0.5Ge0.5) transistors have the lowest drain current. At VDS = 1.2 V, ID curves in this figure can be fitted to the following equations:

$$I_D = (15{,}43x^4 - 28{,}65x^3 + 23{,}28x^2 - 9{,}57x + 2{,}37).\,10^{-4} \quad (1)$$

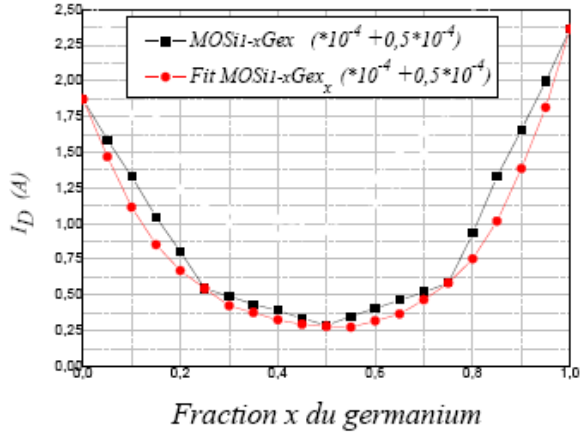
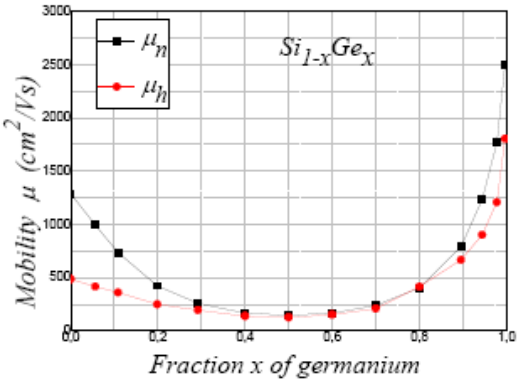


Figure 3. Change of absolute values of ID with Ge fraction x.

Results show that calculated and simulated transistors have good features and functions 16 compared to those in literature [24, 25]. For MOS(Si1-xGex) transistors, the drain current 17 characteristic I_D=f(V_{DS}) is:

$$I_{DS} = U_{eff} C_{ox} \frac{W}{L} \frac{1}{1+V_{DS}/E_{sat}L} \left(V_{gs} - V_{th} - \frac{A_{bulk} V_{DS}}{2}\right) V_{DS} \quad (2)$$

In equation (2), the geometrical channel ratio (W/L) is constant and the type of oxide used is the same for all MOS(Si1-xGex) transistors. Hence, the current is directly proportional to mobility that is responsible for changes in output characteristics. This mobility of electrons and holes in Si1-xGex materials changes with x fraction of germanium. germanium. as shown in Figure 4.



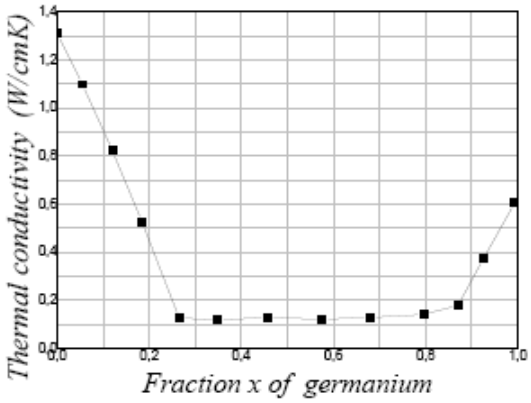


Figure 4: Mobility μn and μh variation in SixGe1-x materials. **Figure 5:** Variation of thermal conductivity of Si1-xGex with germanium x fraction [1].

One way to explain the U-shaped curves ID=f(x) of MOS(Si1-xGex) transistors is that in an alloy, the phonons will experience a greater number of collisions because the lattice sites can be occupied randomly by silicon atoms or germanium. The mean free path of germanium will be lower, thus inducing a less efficient heat transport.

MOS(Si1-xGex) transistors heat up more than silicon ones because of this low heat removal. In turn, this poor heat conduction degrades transistor's electrical properties. Figure 5 shows the variation of thermal conductivity of Si1-xGex with germanium x fraction [1].

Figure 2.b shows that the two functional parts of the transistors in 3C-SiC, 4H-SiC and 6H-SiC technologies are distinct. Ohmic parte (linear) is located for VDS below 0.6V

for 4H-SiC and 6H-SiC based transistors, however for MOS(3C-SiC) transistor, it is up to 1V. The SiC based transistors designed for high voltages and high powers may function well at low voltages and low powers. The MOS(3C-SiC) transistor is characterized by a drain current 5 times greater than that of MOS(6H-SiC) transistor and 15 times greater than that of MOS(4H-SiC) transistor. For BSIM3v3 model the drain current can be expressed as [26]:

$$I_{DS} = \frac{u_{eff} W E_{sat}}{E_{sat} L + V_{DS}} \left(V_{gs} - V_{th} - \frac{A_{bulk} V_{DS}}{2} \right) V_{DS} = a \left(V_{gs} - V_{th} - \frac{A_{bulk} V_{DS}}{2} \right) V_{DS} \quad (3)$$

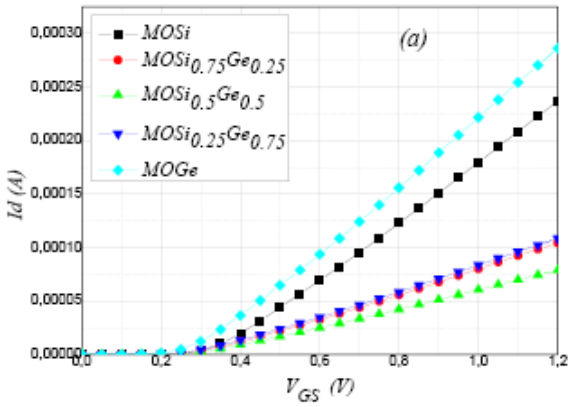
where *μeff* is the effective mobility, *Cox* is the oxide capacitor, *Esat* is the saturation field, *Vth* is the thresh-old voltage and *Abulk* is the parameter of BSIM3v3 model. In expression (3), the ratio a is approximately the same for different transistors because thegeometric structure and oxide type used is the same for the three MOS(SiC) transistors, so the

drain current is inversely proportional to the threshold voltage. Where the threshold voltage *Vth* increases, the expression ($Vgs-Vth-A_{bulk}V_{DS}/2$) decreases and as in SiC technology, Vth ($\boldsymbol{SiC}-3C$) < $Vth(SiC-6H)$ < $Vth(SiC-4H)$, the drain current of MOS(3C- SiC) transistor is greater than the others, as it is illustrated in Figure 6.b. From our results, we conclude that the MOS(4H-SiC) transistor technology is characterized by a low power compared to others (MOS(3C-SiC) and MOS(6H-SiC)) transistors. The band-gap narrowing principle [27-30]. Submicron technology and charge carriers concentration are directly responsible of the operation of our transistors at low voltage and low power. Based on our results, we conclude that the MOS(4H-SiC) transistor is characterized by a low power compared to the other MOS(3C-SiC) and MOS(6H-SiC) transistors.

Since the structure, the dimensions, the doping and the nature of the oxide are identical for all the transistors, then there are only the physical properties (gap, mobility, thermal conductivity, saturation speed, etc.) which impose a difference in the phenomenon of transport. Thus, the drain currents of MOS(SiC) transistors are low compared to MOS(Si1-xGex) transistors.

3.2. ID-VGS Transfer characteristics

To simulate transfer characteristics ID=f(VGS) of MOS(Si1-xGex) and MOS(SiC) transistors, an applied voltage VDS=1.2V was used with VGS voltage varied from 0V to 1.2V. Figure 6 shows the results of simulation.



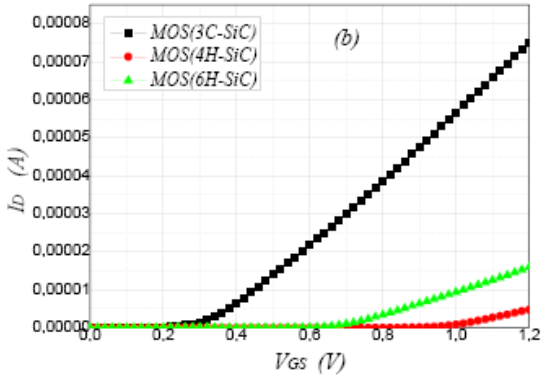


Figure 5: Transfer characteristics ID=f(VGS) of transistors: a) MOS(Si1-xGex) and b) MOS(SiC).

Figure. 6 shows the transfer characteristics ID=f(VGS) at VDS=cte of the MOS(Si1-xGex) and MOS(SiC) transistors. The two operating modes (blocked, linear) are clearly visible on the curves in Figure.6. This allows us to determine the value of the threshold voltage VTh of each transistor as a function of the germanium fraction x for MOS(Si1-xGex), and as a function of the type of polytypes for MOS(SiC).

In the blocked region of operation, the gate-source voltage bias is less than the threshold voltage (VGS <Vth). All MOS(Si1-xGex) and MOS(SiC) transistors have the
same characteristics characteristics and drain currents are very low (ID≈0). These are leakage currents. The MOS(Si1- MOS(Si1-xGex) transistors operation is independent of the x fraction of germanium.

In the linear region, where 0<VGS-Vth<VDS, a gradual increase of VGS (VGS>Vth) leads to an increase in electrons' concentration (n) in the channel. The conductivity of the channel increases according to:

$$\sigma = \eta . q . \mu_n \qquad (4)$$

MOSi1-xGex transistors transfer characteristics are straight lines with the slope *dID/dVGS* changing with x. The parameters affecting these slopes are the carrier concentration n(p) and the mobility µn(µp) (Figure 4) that change with x fraction of germanium. These devices become transconductances (dId/dVgs) controlled by voltage. Results show that MOS(Ge) transistors have a high transconductance compared to the low one of MOS(Si0.5Ge0.5) transistors. It can be used to have a high gain amplifier.
According to Figure 6b, the MOS(4H-SiC) transistor is characterized by a high value of threshold
voltage compared to MOS(6H-SiC) transistor,
and the latter has a threshold voltage higher than the MOS(3C-SiC) transistor.
The geometric structure, oxide type used and doping technology are the same for different MOS(SiC) transistors. The parameters which influence the evolution of threshold voltage of the different MOS transistors by considering BSIM3v3 model (expression 2) [31] are: the carrier concentration n and the gap Eg of each semiconductor.

- Once the gap of semiconductor increases, threshold voltage also increases.

- Once the carrier concentration increases, threshold voltage decreases.

The results obtained show that MOS(SiC) transistors are characterized by higher threshold voltage values compared to

MOS(Si1-xGex) transistors. The dispersion of the values of the threshold voltage of the MOS transistors is largely due to the gap of the Si1-xGex and SiC semiconductors.

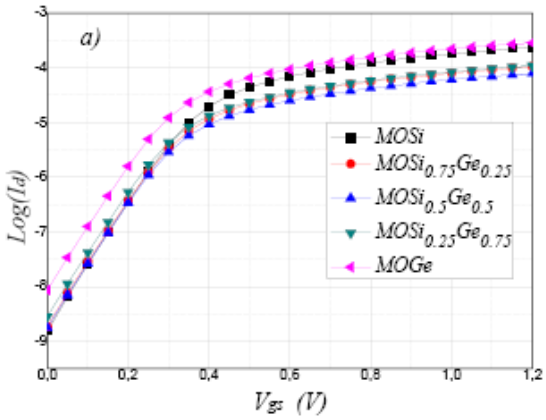
3.3. ION and IOFF Currents

In the model, the ION current and leakage current IOFF are defined by the following relation- ships:

$$I_{ON} = I_D/V_{GS} = V_{DD}, V_{DS} = V_{DD}, V_{bS} = 0 \quad (5)$$

$$I_{Off} = I_D/V_{GS} = 0, V_{DS} = V_{DD}, V_{bS} = 0 \quad (6)$$

The leakage current IOFF is due mainly to the sub-threshold current and to junctions' currents *IjDB* et *IjSB*, while the gate current is negligible. Compared to current IOFF at VGS=0V, I_{gb}, I_{gs} *and* I_{jbs} currents are zero. To do so, the transistor has been biased such as $V_{DS} = V_{DD}$ and $V_{bs} = 0$ (substrate bias) and the curve $Log(I_D) = f(V_{GS})$ has been plotted. Figure 7 shows simulation results.



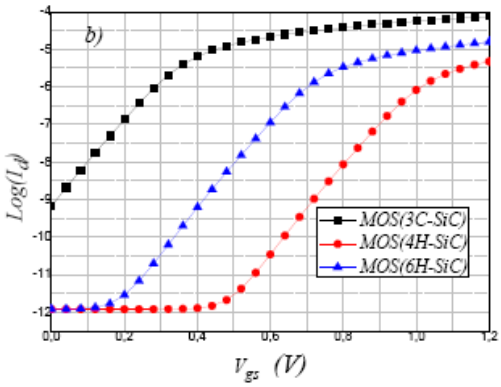


Figure 6: Log(I_D) = f(V_{GS}) characteristics of transistors a) MOS(Si1-xGex) and b) MOS(SiC).

Table 2 shows leakage currents ION and IOFF values obtained from simulation. For the leakage current IOFF, MOS(Si1-xGex) transistors operate in sub-threshold regime. For this regime, the drain current expression is written:

$$I_D = KI_0 \exp\left(\frac{V_{GS}-V_{Th}-V_{off}}{\eta V_T}\right)\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (7)$$

Table 1: Leakage currents ION and IOFF values for MOS(Si1-xGex) and MOS(SiC) transistors

Transistors NMOS	**MOS($Si_{1-x}Ge_x$)**					***MOS(SiC)***		
	Si	Si0.75Ge0.25	Si0.5Ge0.5	Si0.25Ge0.75	Ge	3C-SiC	4H-SiC	6H-SiC
I_{OFF} (nA)	7.89	1.889	1.775	2.850	8.658	0.672	1.99×10^{-9}	7.94×10^{-6}
I_{ON} (mA)	0.237	0.104	$7.881e^{-2}$	0.108	0.286	7.5×10^{-2}	0.475×10^{-2}	1.6×10^{-2}

Since the voltage V_{OFF} is very low, Eq. (7) becomes:

$$I_D = \frac{W}{L} I_0 \exp\left(\frac{V_{GS}-V_{Th}}{\eta V_T}\right)\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (8)$$

With

$$I_0 = u_{eff}\sqrt{\frac{q\varepsilon N_{ch}}{2\Phi_s}}V_T^2 = u_{eff}C_{ox}(\eta-1)V_T^2 \quad (9)$$

The leakage current IOFF is under the influence of two important variables, namely the threshold voltage and carrier mobility. To determine this leakage current, the transistor is biased such as VDS = VDD. In this case, the equation (7) is written taking account of equation (8):

$$I_{OFF} = au_{eff}(\eta-1)\exp\left(\frac{-V_{Th}}{\eta V_T}\right) \quad (10)$$

Where α is given by:

$$a = \frac{WC_{ox}V_T^2}{L}\left(1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (11)$$

The leakage current IOFF of MOS(Si1-xGex) transistors varies with the x fraction of germanium. This variation is very low and is between 1.775nA and 8.65nA. The current ION of MOS(Si1-xGex) transistors varies with mobility and the x fraction of germanium. The effect of the threshold voltage is very low on the variation of this current, as shown in Figure 7.a.

For MOS transistors in SiC semiconductors, the leakage currents IOFF are very low, however that of the MOS(3C-SiC) remains greater than those of the other two (4H-SiC and 6H-SiC)

as shown in Figure 7.b. This last figure shows the evolution of the ION currents of the three MOS(SiC) transistors which are a function of VTh. As the threshold voltage VTh increases, exp(-VTh) decreases and thus ID decreases as VTh increases as shown in Figure 7.b.

From our results, we have shown that the ION and IOFF currents of MOS(SiC) transistors are very low compared to MOS(Si1-xGex) transistors as shown in Figure 7.b and Table 2.

4. Conclusion

The PSpice parameters of MOS(Si1-xGex) and MOS(SiC) transistors with 130 nm technology are calculated and used in simulation under BSIM3v3 software. It has been shown that energy gap, mobility, carrier concentration and velocity saturation are responsible for the evolution of different electronic characteristics of these transistors. Simulations showed that this model of transistors operates with a low voltage of about 1.2 V. They also showed that these transistors operate correctly in a regime sub-threshold and so they can be used in low voltage low power applications. The studied transistors in Si1- xGex and SiC technologies with BSIM3v3 model have yielded very satisfactory results.

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